

What is claimed is:

1. A multi-track speech synthesizer comprising:

a plurality of signal transform units each for receiving a series
5 of digital speech codes and converting them to an
analog speech signal with a zero point at zero and its
negative half-cycles inverted;

a plurality of current switch units each connected to said
signal transform units respectively for receiving said
10 analog speech signal from said signal transform units,
each of said current switch units including a first and
second output terminals to send out a current for
positive half-cycles of said analog speech signal from
said first output terminal and back from said second
15 output terminal and to send out a current for said
negative half-cycles of said analog speech signal from
said second output terminal and back from said first
output terminal;

wherein said first output terminal of each said current switch
20 units connected together to form a first connected
output terminal;

wherein said second output terminal of each said current
switch units connected together to form a second
connected output terminal;

25 a comparison unit for comparing voltages of said first and

second connected output terminals and then sending
out a control signal; and

a current output unit for receiving and sending out currents
from said first and second connected output terminals
from a first and second drive terminals under control of
said control signal from said comparison unit.

2. A speech synthesizer according to claim 1 further
comprising a plurality of volume control units each for receiving a
control signal and producing a control bias to said signal transform
units respectively.

3. A speech synthesizer according to claim 1 wherein each
said signal transform unit controls a conversion of said digital
speech codes by use of a most significant bit of each said digital
speech codes.

4. A speech synthesizer according to claim 3 wherein each
said signal transform unit comprises:

a switched buffer controlled by said most significant bit of said
digital speech codes for receiving and sending rest bits
of said digital speech codes;

a switched inverter buffer controlled by said most significant
bit of said digital speech codes for receiving rest bits of
said digital speech codes and sending out inversion of

said rest bits of said digital speech codes; and
a digital/analog converter connected to said switched buffer
and said switched inverter buffer for converting a
received signal to said analog speech signal.

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5. A speech synthesizer according to claim 3 wherein each
said current switch unit comprises:

a first switched current source for sending out a current
proportional to said analog speech signal to said first
output terminal when said analog speech signal is in
said positive half-cycle;

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a second switched current source for supplying a current
proportional to said analog speech signal to flow in from
said first output terminal when said analog speech
signal is in said negative half-cycle;

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a third switched current source for supplying a current
proportional to said analog speech signal to flow in from
said second output terminal when said analog speech
signal is in said positive half-cycle; and

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a fourth switched current source for sending out a current
proportional to said analog speech signal to said second
output terminal when said analog speech signal is in
said negative half-cycle.

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6. A speech synthesizer according to claim 3 wherein said

current output unit comprises:

5 a first switch with a first terminal connected to said first drive terminal and a second terminal connected to a power supply, said first switch controlled by said control signal from said comparison unit to be conductive when said voltage of said first connected output terminal is higher than that of said second connected output terminal;

10 a second switch with a first terminal connected to said second drive terminal and a second terminal connected to a power supply, said second switch controlled by said control signal from said comparison unit to be conductive when said voltage of said second connected output terminal is higher than that of said first connected output terminal;

15 a fifth switched current source with a first terminal connected to said second drive terminal and a second terminal grounded, said fifth switched current source controlled by said control signal from said comparison unit to supply a current proportional to said current flowing in said second connected output terminal when said voltage of said first connected output terminal is higher than that of said second connected output terminal;

20 and

25 a sixth switched current source with a first terminal connected

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to said first drive terminal and a second terminal grounded, said sixth switched current source controlled by said control signal from said comparison unit to supply a current proportional to said current flowing in said first connected output terminal when said voltage of said second connected output terminal is higher than that of said first connected output terminal.